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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,580	06/26/2003	David William Boerstler	AUS920020690US1	5123

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EXAMINER	
NATALINI, JEFF WILLIAM	

ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 02/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,580	BOERSTLER ET AL.	
	Examiner	Art Unit	
	Jeff Natalini	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) *1-16 and 39-46* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

1. This application contains claims 1-16 and 39-46 drawn to an invention nonelected with traverse in Paper No. 1/21/05. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 17-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Chien et al. (6597249).

In regard to claim 17, Chien et al. discloses a method for testing a phase locked loop (col 6 line 2-17; a lock is determined) having a phase frequency detector (fig 3 (13)) and a voltage controlled oscillator (fig 3 (15)) receiving input from the PFD, and at least one divider receiving input from the VCO (fig 3 (16)) comprising: disabling the PFD (col 3 line 59-60); applying a plurality of test input voltages to the VCO and measuring output frequencies of the VCO as a function of the test input voltages (col 3 line 56 – col 4 line 3); determining lock/capture range of the PLL based on the measured output

frequencies of the VCO as a function of the test voltages (col 6 line 2-8; also see table 1 in col 5, shows voltage inputs VCO_DIN with different outputs); a frequency measuring module for measuring VCO output frequency via the at least one divider and test clock outputs (simulator produces table 1, shows frequency based on VCO_DIV and VCO_DIN-input voltages, VCO_OUT-output of VCO).

In regard to claim 18, Chien et al. discloses performing a minimal set of tests on the PLL based on the lock/capture range of the PLL (abstract, coarse tuning the VCO speeds up the settling time and matches frequencies (col 6 line 5-6), thus verification of the lock/capture range is done easily with fine tuning (col 6 line 9-13).

In regard to claim 19, Chien et al. discloses wherein the test input voltages include discrete DC voltages (col 3 line 61 – col 4 line 3; in order to output different frequencies from the VCO the input voltage must be changed).

IN regard to claim 20, Chien et al. discloses wherein the test input voltages are applied to the VCO through at least one transmission gate (the coarse tuning block shown in fig 4 (contains 22-comparator among others) it is common knowledge in the art that a comparator is made up of transmission gates (MPEP 2144.03)).

In regard to claim 21, Chien et al. discloses an apparatus for testing a PLL (col 6 line 2-17; a lock is determined) comprising: a PLL (fig 3 (13,14,15,16)) having a phase-frequency detector (fig 3 (13)) and a voltage controlled oscillator (fig 3 (15)) receiving input from the PFD; and a test input voltage generator (fig 3 (10)) coupled to the VCO for selectively applying a plurality of test input voltages to the VCO while the PFD is disabled (col 3 line 56 - col 4 line 3).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 22-24, 29-32 and 37 rejected under 35 U.S.C. 103(a) as being unpatentable over Chien et al. (6597249) in view of Huang et al. (Pub 2003/0071748).

In regard to claims 22-24 and 30-32, Chien et al. lacks wherein the voltage generator comprises: N resistors coupled in series between supply voltage and ground/pad, the N resistors forming N+1 nodes between a supply switch and a pad, the supply switch connecting the N resistors to the supply voltage when turned on, wherein N is an integer greater than or equal to 1; N+1 switches being coupled between an input of the VCO and one of the N+1 nodes; a test scan signal generator coupled to the N+1 switches so that a plurality of test scan signals control the N+1 switches when the PFD is disabled; and a scan-enable switch coupled between the N+1 switches and the input of the VCO to be turned on when the PFD is disabled.

Huang et al. discloses a voltage generator comprising N resistors coupled in series between supply voltage and ground/pad (fig 1 (102,106) has 3 resistors),

the N resistors forming N+1 nodes between a supply switch and a pad (fig 1, 4 nodes are seen between supply and ground; also it is known in the art to have a pad on I/O devices to provide a reference voltage (MPEP 2144.03)),

the supply switch connecting the N resistors to the supply voltage when turned on, wherein N is an integer greater than or equal to 1 (fig 1 (112), provides this capability as no voltage is allowed into the amplifier until this switch is closed, no functional advantage is provided in the claimed invention that is not in Huang et al.'s voltage generator by having a switch between the voltage generator and the VCO and a switch between the supply voltage and the first resistor);

N+1 switches being coupled between an input of the VCO and one of the N+1 nodes (Vref15, Vref14, Vref13, Vref0);

a test scan signal generator coupled to the N+1 switches so that a plurality of test scan signals control the N+1 switches when the PFD is disabled (paragraph 11);

and a scan-enable switch coupled between the N+1 switches and the input of the VCO to be turned on when the PFD is disabled (fig 1 (112)).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Chien et al. to have a voltage generator with N resistors between supply and ground forming N+1 nodes between a supply switch and a pad, N+1 switches between an input of the VCO and one of the nodes, a test signal generator, and a scan enable switch as taught by Huang et al. in order to generate stable reference voltages for different stages in a readout chain (paragraph 10).

In regard to claim 29 and 37, Chien et al. does not specifically state input voltage is calculated with the formula Vcc = Vdd/N *m.

The formula to calculate the input voltage: Vc = Vdd/N *m where Vc is the particular test input voltage, Vdd is the supply and m is an arbitrary integer between 0

and N including both 0 and N is obvious from the fig 1 of Huang et al. and basic voltage laws. If the all the resistors are equal and in series (which is the case), each resistor would have a voltage drop of Vdd/N, then you would multiply it by the node to be determined to find the output voltage for a particular node.\

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Chien et al. to use the formula Vc=Vdd/N * m to calculate input voltage as taught by Huang et al. and basic voltage laws in order to correctly find the voltage being supplied.

6. Claims 25-28 and 33-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chien et al. (6597249) in view of Huang et al. (Pub 2003/0071748) as applied to claim 22 and 30 above, and further in view of Sunter (6492798).

Chien et al. as modified lacks wherein at least one of the N+1 switches and the scan enable switch has a transmission gate comprising a p-channel field effect transistor and an n-channel field effect transistor.

Sunter teaches using a conventional CMOS transmission gate (NMOS and PMOS) for a switch (fig 5 (N1,P1; N2,P2); col 8 line 34-35).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Chien et al. as modified to use a CMOS transmission gate as the switches as taught by Sunter in order to improve isolation when the switch is open (col 8 line 34-37).

7. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chien et al. (6597249) in view of Huang et al. (Pub 2003/0071748) as applied to claim 30 above, and further in view of Imai et al. (4851712).

Chien et al. as modified lacks wherein the pad is coupled to an arbitrary input voltage and the supply switch is turned off, and wherein the test input voltage is equivalent to the arbitrary input voltage.

Imai et al. discloses a bias voltage generated by a bias generator and applied to a pad (col 4 line 31-34); also the voltage generator contains pads at different potentials (fig 8 (10,15,16,23)).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Chien et al. as modified to have the pad coupled to an arbitrary input voltage equivalent to the test voltage and have the supply switch off as the pad is supplying voltage as taught by Imai et al. in order to apply a DC bias to an input pulse signal (col 4 line 32-34).

Response to Arguments

8. The objection to the drawling has been removed as the amendment makes it clear the pad can either be grounded or at a lower potential.

Applicant's arguments filed January 21, 2005 have been fully considered but they are not persuasive. In regard to independent claims 17 and 21, Chien et al. discloses determining/measuring the frequencies as a function of the input voltages (col 6 line 2-8 implies this is done; while table 1 in col 5 specifically shows voltage inputs VCO_DIN

with different outputs VCO_OUT, thus showing different frequencies are based on the voltage input into the VCO).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Natalini whose telephone number is 571-272-2266. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lefkowitz can be reached on 571-272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeff Natalini

ANJAN DEB
PRIMARY EXAMINER